

| Course Number | COE328 |
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| Course Title | Digital Systems - F2022 |
| Semester/Year | Fall 2022 |
| Instructor | Shazzat Hossain |
| TA Name | Sajjad |

| Lab/Tutorial Report No. | Lab 2 |
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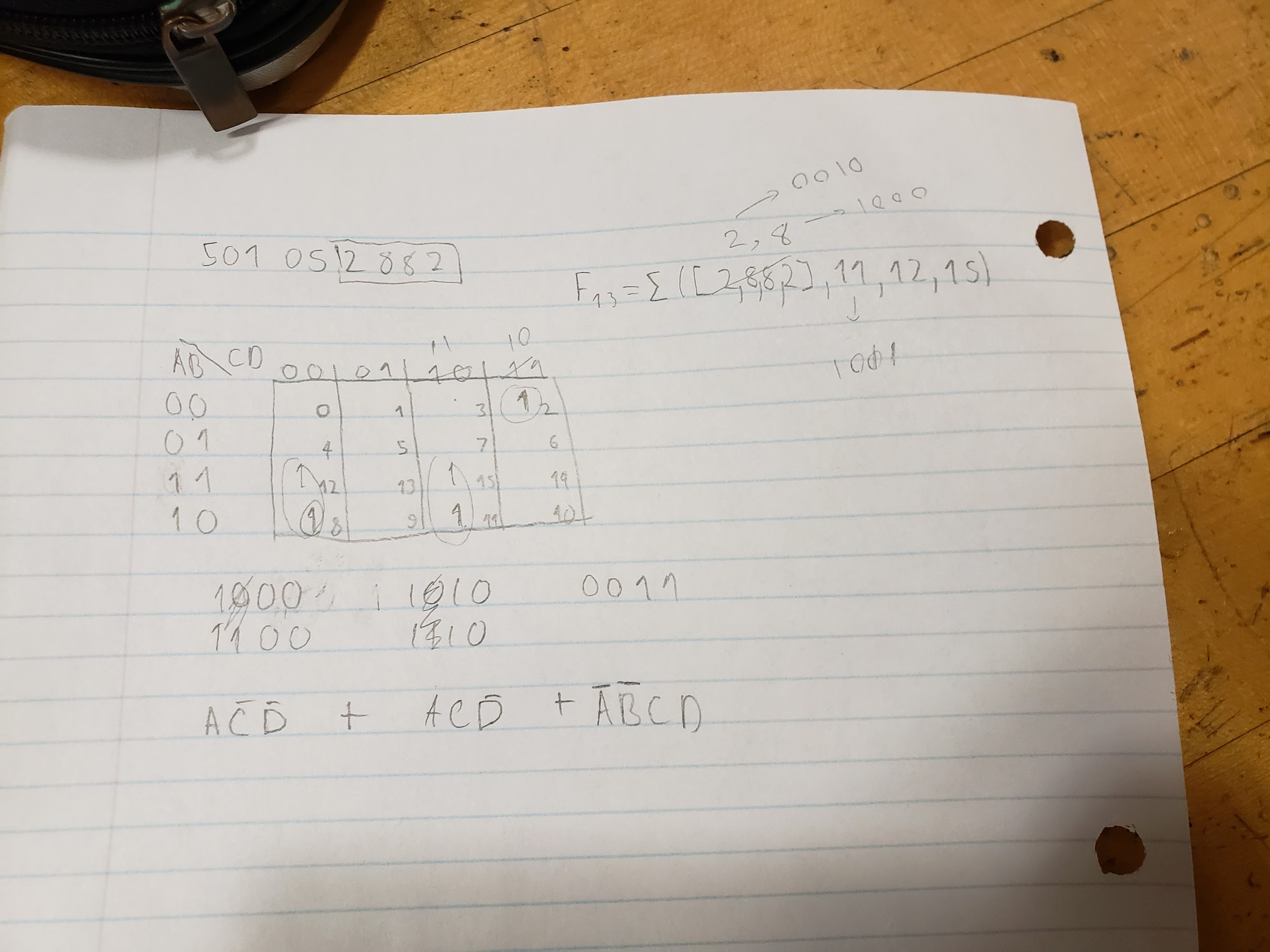
| Report Title | **Function Implementation and Minimization** |
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| Section No. | 11 |
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| Group No. | N/A |
| Submission Date | Oct 2nd, 2022 |
| Due Date | Oct 2nd, 2022 |

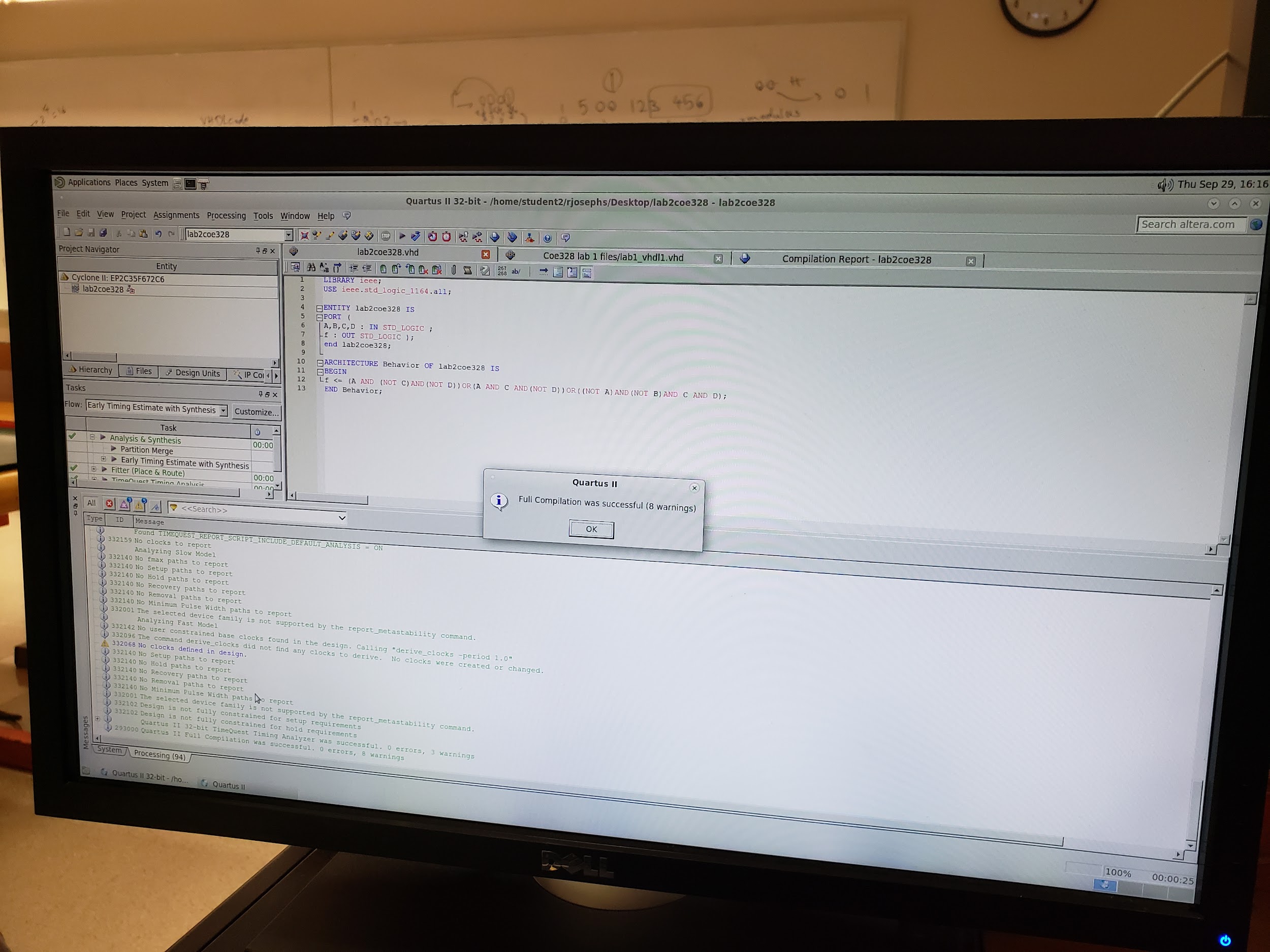
| Student Name | Student ID | Signature\* |
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| [Hamza Malik](mailto:hamza.ejaz.malik@ryerson.ca) | 501112545 |  |

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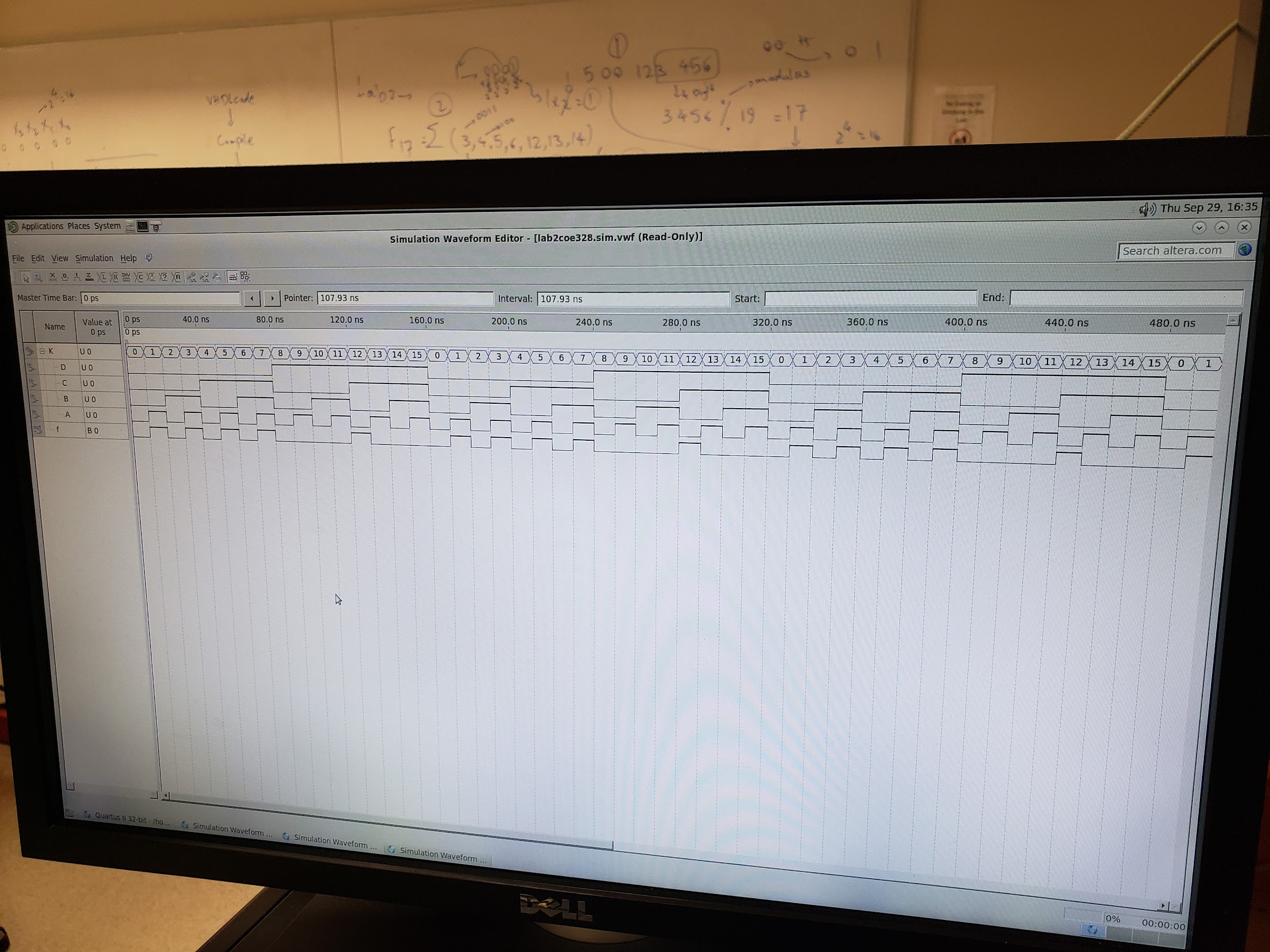
[*http://www.ryerson.ca/content/dam/senate/policies/pol60.pdf*](http://www.ryerson.ca/content/dam/senate/policies/pol60.pdf)



This, is a picture of our k-map with the customized function constructed using my partner's student number during our lab 2 session.



This is our vdhl Skeleton code for lab2coe328 created during our lab 2 with the custom function.



This is a picture of our block diagram schematics. There was an error with the software again, which is why we couldn't get a picture of the proper output. The ta checked our work, and everything is good on our end just, the bug in the software won't provide correct results.

**Conclusion:**

To wrap up our lab 2, we implemented simple logic functions using the Karnaugh map method. In this method, we designed a k-map using the last four digits of our student number, which then got us to the custom function. From that, we wrote our vdhl code with the new custom function and compiled it. After that we designed our diagram schematic with the code to get output f, but unfortunately, there was an error with our software which is why we couldn’t get the right outputs for the block diagram schematics.